Spin Realization of Reversible Logic Gates

Dr. J.Gope (MIEEE, CE)[1] , S.Mondal[2], M.Kundu[3], S.Chowdhury(Kolay)[4]

Abstract— Researchers are facing numerous challenges in designing extremely sophisticated IC's owing to physical limitations of conventional CMOS topology. Conversely incorporation of low power consuming logic is indispensable in modern electronics. These ICs although are not analogous to general ICs (SSI, MSI, and LSI); they are much intended for VLSI or ASIC chips. In this regard Reversible logic h as ushered as a promising computing paradigm having application in low power CMOS, quantum computing, Nano computing and optical computing. Apparently, Nano electronics have made it possible to design Single Spin Logic (SSL) based low dimensional structures to realize high speed low power consuming devices. One such endeavor has been reported here. The authors here tend to mobilize the Single Spin Logic (SSL) topology in realizing Reversible Logic Gate (RLG).

Index Terms— Single Spin Logic (SSL), Reversible Logic Gates (RLG), quantum dot, garbage value, quantum cost, quantum computing and antiferromagnetic

1 Introduction

Moore's law propose that the number of transistors that can be cramped on an integrated circuit should double within the span of 18 months. But this is getting harder and harder to achieve because of inherent physical dimensional constraints of CMOS [1], with the advancement of IC technologies more and more transistor are cramped in same area and the power dissipation increases vigorously which intern enhances the stability and reliability of ICs. Also the conventional charged based logic design produce enormous power dissipation as information is stored at two different charge level. Again the charge is a scalar quantity and has only magnitude. So the logic levels are obtained with only presence or absence of charge. To compensate this, a new methodology that excludes the charge based operation and centers upon spin of an electron evolved and attracted Researchers worldwide. Contradictory spin as a vector possesses fixed magnitude. One can use spin degree of freedom of an electron to realize Boolean Logic. It can be polarized using up spin or down spin generally to achieve the bi-stability. The switching operation can be obtained without manipulating the charge and it considerably reduces the power consumption. The authors here modeled Reversible Logic Gate using this spin logic or single spin logic (SSL) [2], [3].

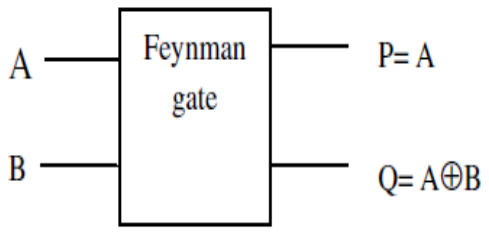
Dr. Jayanta Gope, Chartered Engineer (MIEEE) has received his PhD Degree in Nanotechnology from Jadavpur University, Kolkata and is presently associated with Camellia School of Engineering and Technology. His field of interest includes Nano device modeling, Single Electronic devices, Spintronic Devices, Hybrid CMOS-SET. He has already published around 40+ International research articles in this category. He is nominated as Editorial Board Member and Reviewer of some esteemed Journals and is guiding 6 PhD Scholars in the field of Nanotechnology. He is a life Member of 'CE', 'IEEE-EDS' & 'ISCA'. jayanta.gope.1983@ieee.org
***Mr.Soumitra Mondal**, is a final year student of B.Tech in Electrical and Electronics Engineering Dept. of CSET*
***Ms. Manidipa Kundu**, is a final year student of B.Tech in Electrical and Electronics Engineering Dept. of CSET*
***Mrs. Snigdha Chowdhury (Kolay)** (M. Tech, NITTTR, Kolkata) is associated with Camellia School of Engineering and Technology since 2008. She is continuing her research work in the field of Nano devices under the guidance of Dr. Jayanta Gope.*

2 Reversible Logic Gates

The reversible logic operation is quite pivotal in modern digital logic system as it doesn't loss any information and dissipates very less heat. Contemporarily reversible logic catered much interest in both academia and in industry. Thus designing low power CMOS Reversible gate is very essential. One exclusive application of reversible logic is in quantum computing. The elementary features of reversible gate is that the number of inputs in the reversible circuit is equal to number of output and no fan out is allowed.

In this research attempt, we incorporate three reversible gates- 1) Feynman gate, 2) Toffoli gate, 3) Peres gate and all are realized using single spin logic.

1. **Feynman / CNOT Gate (FG)**: Fig 1 Shows the Single Spin Logic Feynman [5] gate along with its block diagram which is a 2*2 gate and is also called as Controlled NOT. The inputs are A and B and outputs are P=A, Q= A—B. Its Quantum cost is 1. Thus the information processing requires merely 12 electrons whereas CMOS made Feynman gate required minimum 8 transistors. The potentiality of spin logic design is intrinsically obtained from the comparison made above.



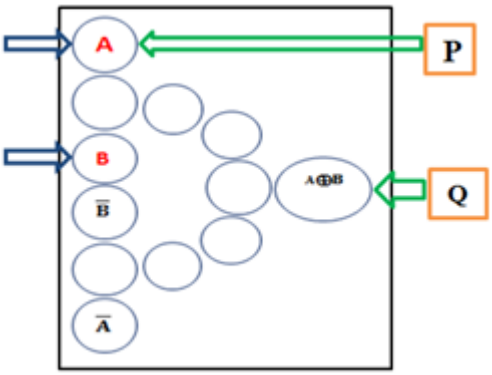
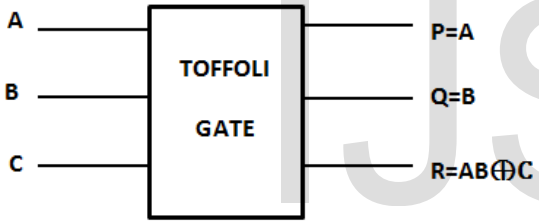


Fig.1 Single spin Feynman gate with its block diagram

2. Toffoli Gate: Fig2 shows a 3*3 Single Spin Logic made Toffoli gate [4]. The inputs are A, B, C and the outputs are P, Q, and R. The outputs are deliberated from P=A, Q=B, R=AB—C. Quantum cost of the Single Spin Toffoli gate is 5. As per the SSL made Feynman gate, the Single Spin Logic Toffoli gate possess all the benefits of Spintronics [5], [6]. One uniqueness is that conventional Toffoli gate comprises of dense wiring whereas Single Spin Logic Toffoli does not involve wiring as spin technology is a wireless technology. This same stands universal truth for any other Single Spin Logic designs.



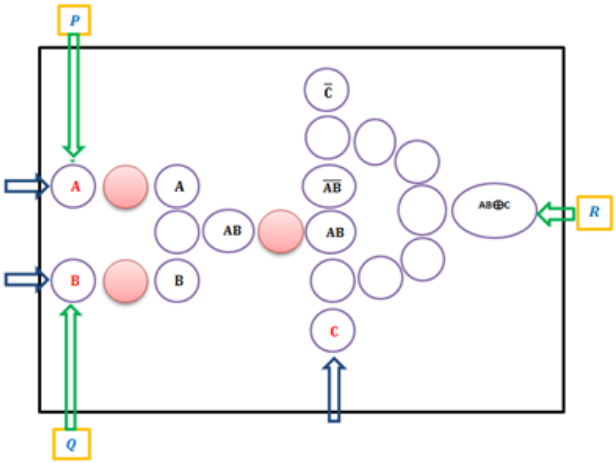
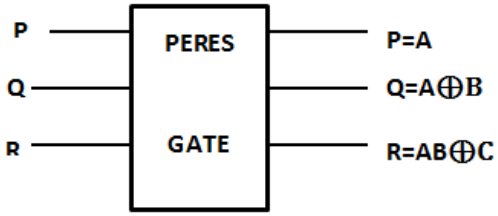


Fig.2 single spin Toffoli gate with its block diagram

3. Peres Gate - Fig3 shows a 3*3 Single Spin Logic Peres gate [7], [8]. The inputs are A, B, C and the outputs are P, Q, and R. The outputs are obtained from P = A, Q = A—B and R=AB—C. Quantum cost of a Single Spin Logic Peres gate is 4. The Single Spin Logic Peres Gate involves 25 spins and that are placed in an antiferromagnetic position with each other. The co-interaction is maintained using the properties of spin degree of freedom.



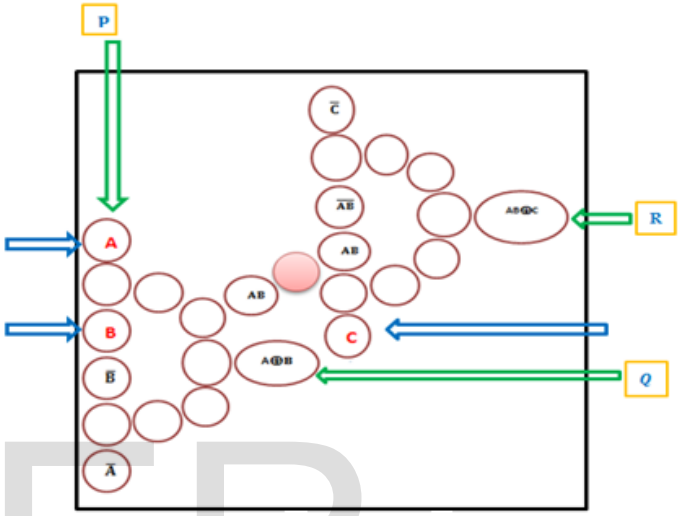


Fig.3 single spin Peres gate with its block diagram

CONCLUSION

Single Spin Logic categorically modified the charge coupling limitations thereby research interest in this category flourished from its very embryonic stage. Here few noteworthy reversible logic gates have been realized using Single Spin Logic. Empirical study revealed that these gates are extra ordinary faster, smaller and are charge independent. Also as their remains no wiring connection the power dissipation drastically reduces. Subsequently the propagation delay improves considerably. Amid such the authors advocate the incorporation of next generation Single Spin Logic based Reversible Logic Gate in quantum computing.

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